Low Voltage Low Power Gilbert Cell based Multiplier Circuit

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Abstract-In this paper a low voltage low power multiplier circuit based on the Gilbert Cell is presented. Spice simulation using 180nm technology is carried out to demonstrate the working of the proposed circuit. Power dissipation of the circuit is 0.0755mW. The -3dB bandwidth of this multiplier is 26.73GHz.

Keywords-CMOS circuit, Gilbert Cell ,high frequency, very low power consumption, modulation.

I. INTRODUCTION

Analog multipliers are extensively used in analog signal processing and communication systems such as mixers in FM receivers[2], amplitude modulators and frequency translators.

Analog voltage multiplication can be performed either by using the square law characteristic of MOS transistors biased in saturation region [3] or by using Gilbert Cell.

The voltage multiplier presented in this work is based on second approach. Since the gain of this cell is a function of control voltage so the output is the multiplication of input voltage and control voltage and hence implement voltage multiplication.

II. CIRCUIT DESCRIPTION

The proposed circuit is based on the Gilbert cell[1],[2],[4]. The property of the Gilbert cell is that the gain of the differential amplifier can be controlled by the tail current. Fig.1 shows the architecture of the proposed multiplier.

In this circuit, transistor MP1, MP2 and MP3 act as a current mirror. The current mirror is used to provide the active load. Transistor MP4 is a diode connect

MOSFET act as a resistance. Transistor M1, M2, M3, M4, M5 and M6 form the Gilbert Cell architecture. M7 and M8 are the bias transistors, used to provide the constant current.

All the transistor operates in saturation region. The condition to keep the transistor in saturation is that:

$V_{DS} \geq V_{GS} - V_{TH}$

where V_{GS} is gate to source voltage, V_{DS} is drain to source voltage and V_{TH} is threshold voltage.

Current through the transistor in saturation is given by:

$$I_D = \frac{1}{2}K(V_{GS} - V_{TH})^2 \qquad (1)$$

where $K = \mu_0 C_{OX} \frac{W}{L}$, μ_0 is mobility, C_{OX} is gate oxide capacitance, W is channel width and L is the channel length.

From the fig.1 the following equation for transistor M5 & M6 can be written as

$$V_{C1} - V_{C2} = V_{GS5} - V_{GS6} \qquad (2)$$

When the transistor operates in saturation then from equation (1) :

$$(V_{GS} - V_{TH})^2 = \frac{I_D}{\frac{1}{2}\mu_0 C_{OX}\frac{W}{L}} = \frac{2I_D}{K} \qquad (3)$$

For transistor M1 & M2, M5 & M6:

$$V_{GS1} = \sqrt{\frac{I_{D1}}{K}} + V_{TH} \qquad (4)$$

$$V_{GS2} = \sqrt{\frac{I_{D2}}{K}} + V_{TH} \qquad (5)$$

$$V_{GS5} = \sqrt{\frac{I_{Ds}}{K}} + V_{TH} \quad (6)$$

$$V_{GS6} = \sqrt{\frac{I_{Ds}}{K}} + V_{TH} \quad (7)$$

$$V_{C1}- V_{C2} = \sqrt{\frac{I_{Ds}}{K}} - \sqrt{\frac{I_{Ds}}{K}} \quad (8)$$

$$(V_{C1}- V_{C2})^2 = \left(\sqrt{\frac{I_{Ds}}{K}} - \sqrt{\frac{I_{Ds}}{K}}\right)^2$$

Putting the value of V_{GS5} & V_{GS6} in eq. (2) and squaring. It gives

$$2\sqrt{I_{DS}I_{D6}} = I_{SS} - \frac{K}{2}(V_{C1}- V_{C2})^2$$

Again squaring on both sides:

$$\left(2\sqrt{I_{DS}I_{D6}}\right)^2 = \left(I_{SS} - \frac{K}{2}(V_{C1}- V_{C2})^2\right)^2$$

$$I_{DS} - I_{D6} =$$

$$(V_{C1}- V_{C2}) * \frac{K}{2}\sqrt{\frac{4I_{SS}}{K} - (V_{C1} - V_{C2})^2} \quad (9)$$

Similarly for transistor M1 & M2, M3 & M4:

$$I_{D1} - I_{D2} =$$

$$(V_1- V_2)\frac{K}{2}\sqrt{\frac{4I_{Ds}}{K} - (V_1 - V_2)^2} \quad (10)$$

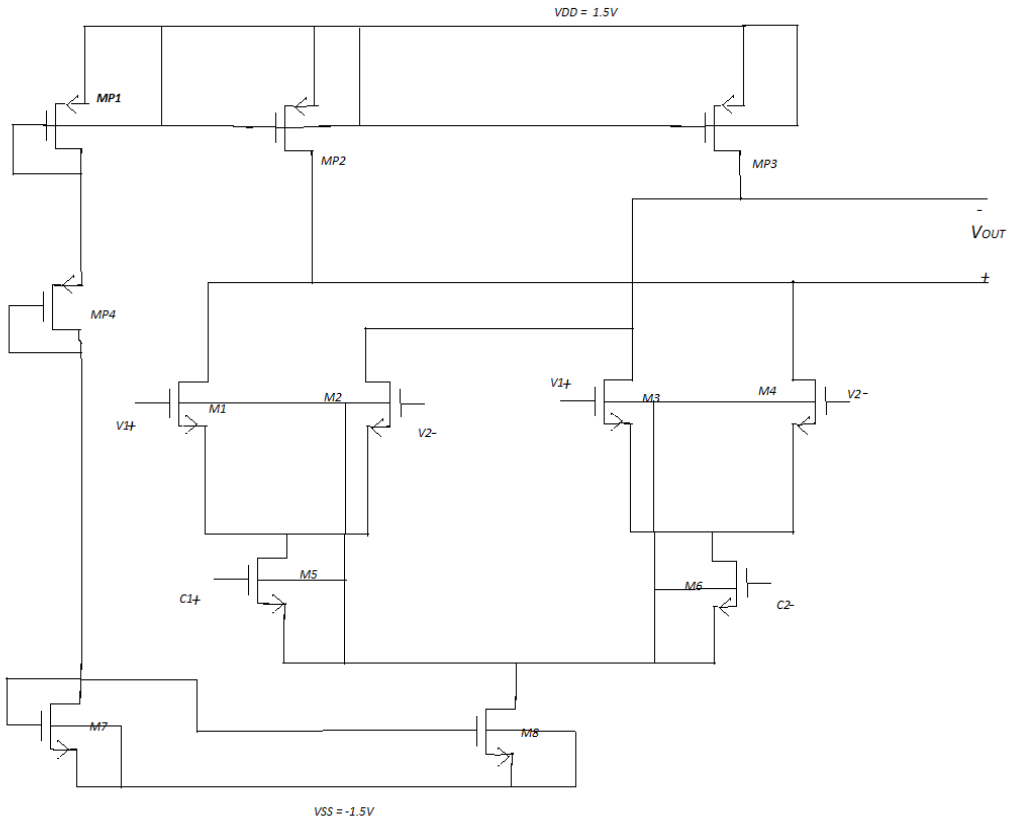


Fig.1 Proposed Multiplier Circuit

$I_{D3} - I_{D4}$=

$(V_1 - V_2)\frac{K}{2}\sqrt{\frac{4I_{D5}}{K} - (V_1 - V_2)^2}$ (11)

Since the signal is applied in the complementary form, so:

V_1=-V_2=V_1 & V_{C1}=-V_{C2}=V_C

The input signal being very and $(V_1)^2$ can be approximated to zero.

Thus eq. (10) & (11) reduce to:

$I_{D1} - I_{D2} = V_1\sqrt{4KI_{D5}}$ (12)

$I_{D3} - I_{D4} = V_1\sqrt{4KI_{D6}}$ (13)

2.1 The output voltage(V_{out})

Output is taken at the drain of transistor M1 &M3.So output V_{OUT} can be written as:

$V_{OUT} = R_D(I_{D1} - I_{D2} + I_{D3} - I_{D4})$

$V_{OUT} = R_D V_1(\sqrt{I_{D5}} - \sqrt{I_{D6}})\sqrt{4K}$ (14)

Where R_D is the resistance provided by the active load.

From eq. (8) putting the valve of $(\sqrt{I_{D5}} - \sqrt{I_{D6}})$ in eq. (14)

$V_{OUT} = R_D V_1(V_{C1} - V_{C2})\sqrt{4K * \frac{K}{2}}$ (15)

since V_{C1}=-V_{C2} = V_C so from eq. (15)

$V_{OUT} = C * V_1 * V_C$

Where $C=2 R_D K$

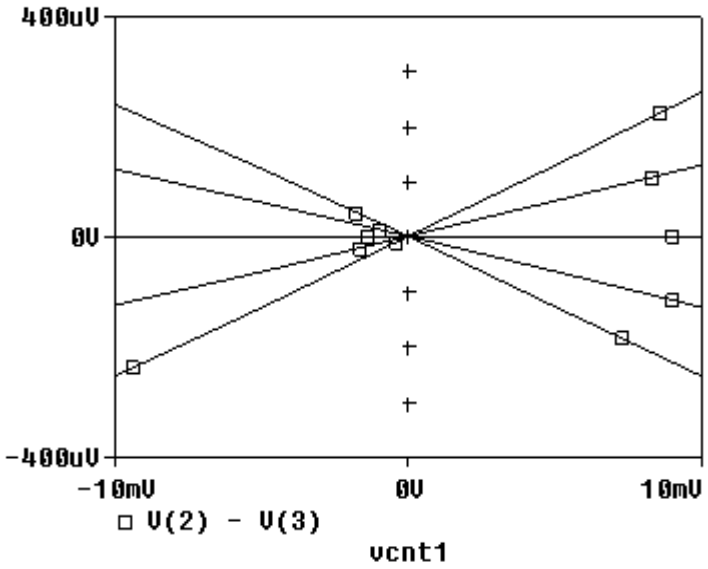
This clearly shows that V_{OUT} is multiplication of input voltage and control voltage.

III. Simulation Results

Proposed circuit is verified through PSPICE simulation. SPICE simulation was performed using .18um CMOS process parameter provided by Mosis. Supply voltage used were ±1.5V. The simulation result shows that its frequency response is 26.73 GHz. Its power dissipation observed is 0.0755mW.

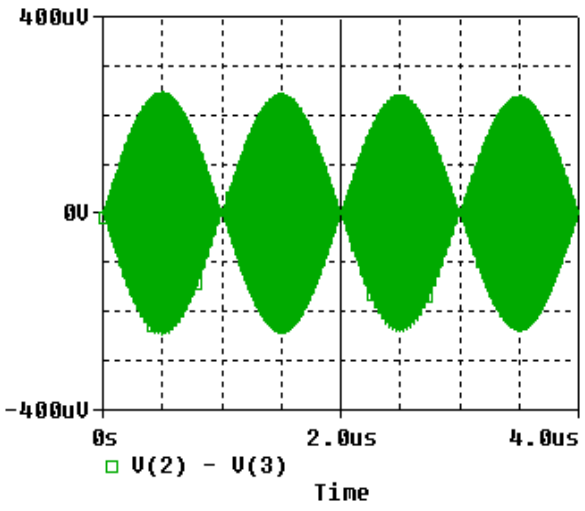
A. DC Response

Fig.2 shows the DC response of the proposed circuit. For ±10mV input signal voltage, the output voltage swing is ±250uV.



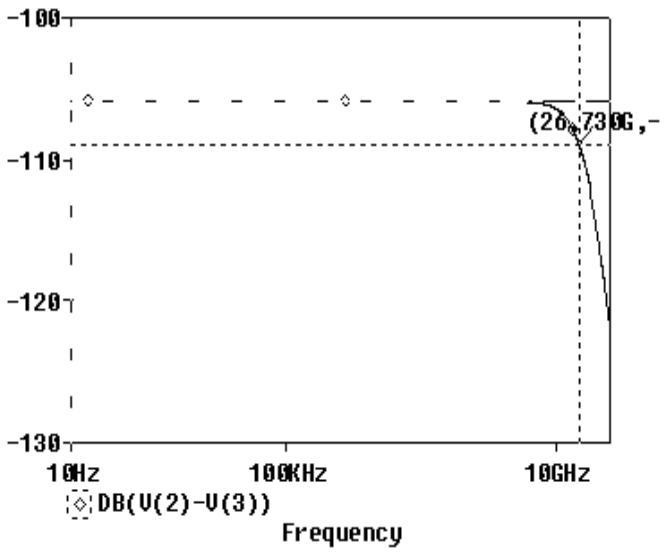
B. Transient Response

Fig.3 shows the transient response of the proposed multiplier circuit as an amplitude modulator. Here the frequency of the modulating (V_1) and the career (Vc) signals are 500KHz and 0.1GHz sinusoidal with peak amplitude of 10mV .



B. AC Response

Fig.4 shows the AC response of the proposed multiplier circuit. The -3dB bandwidth of this multiplier is 30.2GHz.



IV. CONCLUSION

A low voltage and low power Gilbert Cell based multiplier has been proposed. The proposed circuit can operate at ±1.5v power supply. The circuit is simulated on SPICE using level 7 model parameter CMOS 180nm technology. Simulation result shows, the DC to DC voltage swing is ±134mv, -3db frequency response is 26.73GHz and power dissipation is .0755mW.

ACKNOWLEDGEMENT

We express our sincere gratitude to Mrs. Rajeshwari Pandey, Associate Professor, Electronics & Communication Department, D.T.U. ,New Delhi for her support, comments and technical assistance.

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